Communication Products: Frequently Asked Questions

This FAQ discusses answers to general communication questions as well as Dallas Semiconductor device-specific questions.

This FAQ is designed to address some of the more common questions that will arise when using Dallas Semiconductor Telecommunication devices in new or existing designs. The questions are divided into different categories based on a specific information areas. Because some devices like the DS2155 have a combination of features, it is possible that questions related to the DS2155 will span multiple categories.

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1. General Telecommunication Questions

Q1. In T1 what is the difference between Superframe (SF) / D4 and Extended Superframe (ESF)?

A1. While both formats contain the same number of channel time slots, the SF format is a 12 frame structure while ESF contains 24 frames. Both use the 8th bit of each channel time slot in every 6th frame for signaling, thus providing the SF format with A/B signaling bits and the ESF format with A/B/C/D signaling bits every multiframe. Also, the ESF format uses the F bits to provide frame alignment, CRC-6 check bits, and a 4 kbit/s data link. The SF format divides the F bits into Ft and Fs bits. The Ft bits are terminal framing bits which identify frame boundaries and the Fs bits are signaling framing bits which identify signaling frames.

Q2. What is the difference between T1 and E1?
A2. The main differences in T1 and E1 are the operating frequency, the number of time slots, the pulse shape, the characteristic line impedance, and the signaling method. The T1 system operates at 1.544 MHz with a total of 24 time slots. The T1 pulse shape contains over and under shoot and is driven on a line impedance of 100Ω. Finally, digital messages to signal on and off hook or other conditions are sent using robbed bit signaling. The E1 system operates at 2.048 MHz with a total of 32 time slots. The E1 pulse shape is a perfectly rectangular pulse shape and is driven on a line impedance of 120Ω or 75Ω. Finally, digital messages to signal on and off hook or other conditions are sent using channel associated signaling.

Q3. What is the difference between T1 and J1?
A3. The J1 term is commonly used to refer to the derivation of the North American T1 standard that is used exclusively in Japan. Differences exist between J1 and T1 in the Yellow Alarm generation for Super Frame (SF) and Extended Super Frame (ESF) modes. Also, the CRC-6 calculation in Extended Super Frame mode is different. In J1 Super Frame mode, the Yellow Alarm is generated when a '1' is transmitted in the 12th F-bit as opposed to T1 Super Frame mode where a '0' is transmitted in the 2nd bit of all timeslots. In J1 Extended Super Frame mode, the Yellow Alarm is generated by transmitting 'FFFF' in the data link (DL) section of the F-bits, versus T1 Extended Super Frame mode where 'FF00' is transmitted in the data link. In J1 Extended Super Frame mode the CRC-6 calculation includes the Frame Alignment Signal and Data Link F-bits. However, for T1, all of the F-bits are set to '1' when the CRC-6 calculation is performed.

Q4. What is SLC-96 and how does it relate to T1?
A4. SLC-96 (pronounced "slick 96") is used in conjunction with T1 as a digital loop carrier system which provides service for up to 96 subscribers over 3 to 5 separate T1 lines. SLC-96 was the first widely deployed digital loop carrier system. SLC-96 operation consists of two terminals, a Central Office Terminal (COT) and a Remote Terminal (RT). The Central Office Terminal multiplexed the analog phone lines from a class 5 switch into four T1 lines with an optional fifth T1 line used for protection switching. The Remote Terminal was the termination point for the T1 lines and converted them into subscriber phone lines. SLC-96 revolutionized the telecom industry by introducing digital electronics into the local loop as a permanent replacement for cable. The frame format of SLC-96 closely resembles that of the super frame (SF or D4) format except that additional data link information is transferred in the framing bits. This allows the deployment of advanced functions such as single party, multiparty, coin telephone, and special service circuits. For more information on SLC-96 please consult Telcordia specification TR-008.

Q5. How are frames, channel time slots, and bits numbered in T1 and E1?
A3. According to the ITU-T specification G.704 the numbering structures for T1 and E1 digital transmission systems is as follows.

In T1 systems, the frames are numbered 1 - 12 in the Superframe (SF) / D4 format, and 1 - 24 in the Extended Superframe format (ESF). The channel time slots are numbered 1 - 24. The bits

are numbered 1 - 8 with the 8th bit being the least significant bit.

In E1 systems, the frames are numbered 0 - 15 in the CRC-4 and CAS multiframe format. The channel time slots are numbered 0 - 31. The bits are numbered 1 - 8 with the 8th bit being the least significant bit

Q6. What is the difference between Robbed Bit Signaling (RBS), Channel Associated Signaling (CAS), and Common Channel Signaling (CCS)?

A6. RBS is the original signaling system used by T1 and provides either 2 or 4 signaling bits per channel depending on the multiframe format. In RBS, the least significant bit in every channel of every 6th frame is used as a signaling bit. Hence, in the SF format there is an A/B and in the ESF format there is an A/B/C/D bit for every channel. CAS is the original signaling system used by E1 and provides 4 signaling bits for every channel. In CAS, channel 16 is reserved for signaling and the A/B/C/D bits for each channel are divided among 16 frames. Frame 0 contains the alignment signal, alarm, and spare bits. Frame 1 contains the A/B/C/D bits for channel 1 in the upper half of the channel and the A/B/C/D bits for channel 16 in the lower half. The remaining 14 frames follow the frame 1 format accordingly. In recent years, the term RBS has been replaced by CAS which is now used to refer to bits that are associated with a specific channel whether it is in the T1 or E1 format. CCS is used by either T1 or E1 and refers to a system that does not use a specific bit structure for signaling. Instead, all or part of a channel is used to pass messages between two systems to indicate how a channel is being used. This type of system is commonly found in ISDN which uses a D channel to pass messages.

Q7. What are the Red, Blue, and Yellow alarms in a T1 system?

A7. The three different alarms are used to indicate different problems in the transmission or reception of data in the T1 system. To explain the different alarms it is necessary to have a simple T1 system model that has a T1 signal sourced from the Central Office (CO) through a Repeater to the Customer Premises Equipment (CPE) and back. The Red alarm is actually a state that the CPE is in from the detection of an incoming signal failure (i.e. from a line break). The Yellow alarm is transmitted to indicate the loss of an incoming signal. In the case where the CPE is in the Red alarm state, it will transmit the Yellow alarm to the Repeater. The Blue alarm is transmitted upon loss of the originating signal or when a signal is actively disrupted. In the case where the Repeater receives the Yellow alarm, it will transmit the Blue alarm back to the CO. Upon receiving a Blue alarm, the CO will transmit a Yellow alarm to the Repeater to indicate the loss of incoming signal. It may seem confusing as to whether a piece of equipment should transmit a Yellow or Blue alarm. Generally, any piece of equipment on the endpoint (i.e. CPE or CO) will transmit the Yellow alarm to indicate the loss of signal while equipment in the middle of the path (i.e. Repeater) will transmit the Blue alarm.

Q8. What are the Alarm Indication Signal (AIS), Remote Alarm Indication (RAI), and Distant Multiframe Alarm (DMA) in an E1 system?

A8. The AIS and RAI are essentially the same as the T1 Blue and Yellow alarm respectively. The AIS is transmitted upon loss of the originating signal or when the incoming signal is actively disrupted. The RAI is transmitted to indicate the loss of an incoming signal. The DMA is specific

to CAS signaling and is transmitted when the correct CAS multiframe alignment signal is not found.

Q9. What is the difference between AMI, B8ZS, and HDB3?
A9. AMI, B8ZS, and HDB3 are different types of line coding used in T1 and E1 communications systems. AMI stands for alternate mark inversion and is used in both T1 and T1 systems. B8ZS stands for Bipolar with 8 Zeros Substitution and is used in T1 systems while HDB3 stands for High-Density Bipolar 3 and is used in E1 systems.

AMI is the most basic encoding scheme, where ones are represented by voltage pulses and zeros are represented by the lack of a voltage pulse. In AMI, the polarity of each pulse is the opposite of the previous pulse. The problem with using AMI is that if not enough voltage pulses are sent down the line, then the receiver will not correctly decode the data stream. To solve this problem, two different encoding schemes were developed to replace a sequence of zeros with a special code word of voltage pulses. The B8ZS encoding scheme replaces each sequence of 8 zeros with the code of 000VB0VB, where the V pulse (bipolar violation) has the same polarity as the previously pulse and the B pulse (correct bipolar pulse) has the opposite polarity as the previous pulse. HDB3 encoding is slightly more complicated because unlike the B8ZS encoding which has a balance of positive and negative voltage pulses, the HDB3 encoding has to select a code word to maintain the balance. In HDB3 each sequence of 4 zeros is replaced by 000V or B00V. The decision of which code word to use is made so that the number of B pulses between consecutive V pulses is odd. This maintains the balance of positive and negative pulses when using HDB3 encoding. The table below has examples of the different encoding types.

Data	0	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1
AMI	0	+	0	−	+	0	0	0	0	0	0	0	0	−	0	0	+	0	0	0	0	−
B8ZS	0	+	0	−	+	0	0	0	+	−	0	−	+	−	0	0	+	0	0	0	0	−
HDB3[1]	0	+	0	−	+	0	0	0	+	−	0	0	−	+	0	0	−	+	0	0	+	−

Figure 1. The previous V bit is directly before the beginning of the data sequence.

Q10. What are the names for the regulatory bodies that govern the requirements for the network interface line protection?
A10. There are many different regulatory bodies that govern how the T1 and E1 line interfaces must operate under surge and power cross conditions. The list below contains the commonly referenced regulatory bodies and the specifications that apply in each case.

FCC Part 68: Effective July 23, 2001, the Administrative Council for Terminal Attachments (ACTA) assumed operational responsibility for Part 68. ACTA is the newly-formed industry council for Part 68 certification requirements and administration following the FCC's decision to privatize its Part 68 responsibilities and selected TIA and ATIS to serve as joint sponsors of the Council. Because of this, FCC Part 68 has been renamed to TIA/EIA-IS-968.

Old Part 68 URL: http://www.fcc.gov/wcb/iatd/part_68.html

New Part 68 URL: http://www.part68.org

UL 1950: Underwriter Laboratories has made changes to the naming of the over voltage specifications which was known as UL 1950, 3rd edition. This specification has now been renamed to UL 60950, 3rd Edition.

Old UL1950 URL: http://www.ul.com/pag1950
New UL60950 URL: http://data.ul.com/pagos

Q11. What is the difference between jitter and wander?
A11. Jitter is defined as the magnitude of phase variation (with respect to a reference clock or data signal), whose frequency of variation is greater than 10 Hz. Jitter is measured in Unit Intervals (UI), where 1 UI is equal to one data bit-width. For an E1 signal, 1 UI is equal to 488 ns, and for a DS1 signal, 1 UI is equal to 648 ns. However, if the rate of change in phase is less than 10 Hz, then this phenomenon is known as wander, and is measured in nanoseconds.

Q12. What standards bodies govern telecommunications equipment compliance?
A12. The following is a list of the largest telecommunications standards bodies:

- American National Standards Institute - ANSI (www.ansi.org)
- European Telecommunications Standards Institute - ETSI (www.etsi.org)
- International Telecommunication Union - ITU (www.itu.int)
- Telecommunication Technology Committee - TTC (www.ttc.or.jp)
- Telecommunications Industry Association - TIA (www.tiaonline.org)
- Telcordia Technoligies Incorporated - Telcordia (www.telcordia.com)
- Underwriters Laboratories Incorporated - UL (www.ul.com), UL Europe (www.ul-europe.com)

2. General Device Operation Questions

Q1. What is the standard register settings for a certain Dallas Semiconductor device?
A1. Since there are many different ways that a T1, J1, E1, T3, or E3 device can communicate, there are no standard register settings. After initialization, there are 3 register types that control all major device operations. These are the Receive Control Registers (RCRx), the Transmit Control Registers (TCRx), and the Common Control Registers (CCRx).

Q2. What software is available for use with Dallas Semiconductor devices?
A2. Software drivers are available for the following T1/E1 devices:
DS2152, DS2154, DS21(Q)352, DS21(Q)552, DS21(Q)354, DS21(Q)554, DS21(Q)55, DS21455, and DS21458.

Software drivers are available for the following T3/E3 devices:
DS3112, DS3141, DS3142, DS3143, DS3144, DS3151, DS3152, DS3153, and DS3154.

The drivers are written in C and supplied by Ncomm. The drivers may be obtained by submitting an email request to the following address telecom.support@dalsemi.com. Please note that company contact information will be necessary before the request can be processed.

Q3. Can you provide an example design using various processors?
A3. There are several example designs using processors by various manufacturers located in the Design and Applications section of the Maxim website at www.maxim-ic.com. Just click on Application Notes by Categories link and then on the Communication Circuits link.

Q4. Can you provide a reference design for the network interface?
A4. Application note 324 provides all the information required to implement the network interface and is located in the Design and Applications section of the Maxim website at www.maxim-ic.com. Just click on Application Notes by Categories link and then on the Communication Circuits link.

Q5. What do the markings on Dallas Semiconductor devices stand for?
A5. Example Markings for the DS2149 28 Pin PLCC Package

DALLAS
DS2149 - Device
YYWWRR - Date code
###XX - Lot code

Date Code:
YY - Last two digits of the year of assembly
WW - Week within the year of assembly
RR - Revision

Lot Code:
- Last three digits of the lot number
XX - Up to two alpha characters that are behind those digits

Q6. What is the difference between the device identification register (IDR) value and the device revision markings on Dallas Semiconductor devices?
A6. The device revision, printed on the top of the package consists of a alphanumeric combination two characters in length. The alpha character denotes the current level of a all layer die revision with the first die being denoted with the letter 'A'. The numeric character denotes the current level of a metal layer die revision with the first die being denoted with the number '1'. If only the metal layers of the die are revised, then the numeric portion is increased by one. When all the layers of the die are revised, then the alpha portion is increase by one letter and the

numeric portion is returned to the number '1'. Further changes follow the same standard.

For all Dallas Semiconductor T1/E1 devices with an 8 bit data bus, the device identification register (IDR) is eight bits in length and have the following format. The upper four bits used to identify the device family for example, the DS2155, DS21354, DS21552, etc. The lower four bits are used to identify the specific revision of the die. Since the lower four bits can not denote the same alphanumeric combination as printed on the device, the binary value is simply increase by one when any revision is made to the die with the value of '0000' indicating the 'A1' revision. It should be noted that some Dallas Semiconductor device have a 16 bit data bus and follow a different identification register model detailed in the specific device data sheet.

3. Framer / Single Chip Transceiver Related Questions

Q1. How are the DS21x5y, DS215y, or other telecommunication devices initialized?
A1. Some devices like the DS2155 T1/E1 Single Chip Transceiver or DS2148 Line Interface Unit offer a power on reset and a hardware reset pin which clears out all the registers. The other devices will require the software to write a 0x00 to address space 0x00 to 0xFF regardless of register type or documented presence. This ensures that all of the registers are cleared and the device is in normal operation mode.

Q2. Do Dallas Semiconductor devices support unframed or transparent mode operation?
A2. Yes. A description of how to configure a device for unframed or transparent mode operation is provided in application note number 336. This application note is located in the Design and Applications section of the Maxim website at www.maxim-ic.com. Just click on Application Notes by Categories link and then on the Communication Circuits link.

Q3. Is it necessary to repeat the same data on the TSIG pin for an entire multiframe when using hardware based signaling?
A3. Yes. The chip is designed to expect signaling data during the least significant nibble during all timeslots and all frames of a multiframe. Failure to do so will cause unstable results.

Q4. How are JTAG functions implemented on the Single Chip Transceiver multi-chip modules such as the DS21Q352 or DS21Q55?
A4. The term multi-chip module is used in reference to any device that contains multiple die or devices housed in the same package. The DS21Q352, DS21Q354, DS21Q552, DS21Q554, and DS21Q55 are all examples of quad port, single chip transceiver, multi-chip modules. Each of these multi-chip module has four single port devices with daisy chained JTAG functionality. This is necessary because each single port device contains a JTAG test access port controller and the BSDL language lacks the ability to define multiple test access port controllers. In the module, some pins such as address and data buses are tied together. The JTAG pins are either tied in parallel or daisy chained as appropriate. More detail can be found in the device data sheets. To create the proper JTAG scan chain, four copies of the single port version of the device need to be placed in the JTAG chain. If a DS21Q55 were placed on the board, the proper

BSDL file would be the DS2155.

When using the multi-chip modules in the JTAG chain, the design may need to be modified slightly to reflect the internal connections present in the module. How much modification needs to be done will depend on whether the module is being used on physical tester or in conjunction with a simulation program. If the module is being used on a physical board, then the implementation will only require that four copies of the single port BSDL file to be placed sequentially in the JTAG test chain. If however, the module is being used in a simulation the implementation may be slightly more complex. The first way to create a useful simulation model is to create a hierarchy in the design. The quad port module is considered to be a separate board made of four single port devices. The connections are then made to match those present inside of the module itself, these connections are detailed in the device data sheet. Another way is to directly alter the netlist after the design is complete. This will essentially trick the simulation into believing that the quad port module is four separate single port devices.

BSDL files are located at www.maxim-ic.com in the Designer's Information section.

Q5. Is DS2155 pin compatible with other Dallas Semiconductor Single Chip Transceivers?
A5. The DS2155 is closely pin-compatible with DS2152/54, DS21552/554, and DS21352/354 Single Chip Transceivers. The biggest difference between the DS2152/54, DS21552/554 and the DS2155 or DS21352/354 devices is that the former devices all operate on 5.0 volts while the latter operates on a 3.3 volts (with 5.0 volt I/O tolerance). The DS2152/54 devices also do not support many of the pins/functions that the DS2155 has available. The DS21552/554 and DS21352/354 offer the best compatibility but there are some pins/functions that were changed between the DS21x5y and the DS2155. The table below notes all the differences between the pins of the parts.

Pin	Part			
	DS2152/54	DS21552/554	DS21352/354	DS2155
Supply Voltage	5.0	5.0	3.3	3.3
Pin 2	NC	JTMS	JTMS	JTMS
Pin 3	8MCLK	8MCLK	8MCLK	BPCLK
Pin 4	NC	JTCLK	JTCLK	JTCLK
Pin 5	NC	JTRST	JTRST	JTRST
Pin 7	NC	JTDO	JTDO	JTDO
Pin 8	NC	NC	NC	UOP0
Pin 9	NC	NC	NC	UOP1
Pin 10	NC	JTDI	JTDI	JTDI
Pin 14	TEST	TEST	TEST	TSTRST
Pin 15	NC	NC	NC	UOP2

Pin 23	NC	NC	NC	UOP3
Pin 36	NC	CI	CI	ESIBS0
Pin 54	NC	CO	CO	ESIBS1
Pin 76	NC	FMS	FMS	ESIBRD

Q6. Do the Dallas Semiconductor T1 devices support SLC-96?
A6. Because of the complexity of the SLC-96 specification, special synchronization circuitry, data registers, and status registers were added to the T1 devices which allow the system designer to take advantage of the SLC-96 functionality. Dallas Semiconductor T1 devices like the DS2141A, DS2151, DS2152, DS21352, DS21552 and DS2155 are capable of SLC-96 operation in both the transmit and receive direction. On the receive side, the devices are able to synchronize onto a received SLC-96 pattern and extract the message bits. On the transmit side, the devices are able to insert the SLC-96 synchronization pattern and message bits. The devices also have the option to perform the SLC-96 functions either externally through hardware pins or internally through software registers and interrupts.

Q7. What are some common problems and solutions when using the internal DS2155 HDLC?
A7. The DS2155 single chip transceiver contains two high level data link controllers (HDLC). The device has the ability to transmit and receive packet data over a T1/E1 or J1 line. Each controller in the DS2155 can be configured for use with time slots, Sa bits (E1 mode), or the FDL (T1 mode). Each controller has a 128-byte FIFO in the transmit and receive path.

The most common problems are receiving incorrect data in the packets, not receiving enough data bytes in the packets, or receiving an prematurely terminated (aborted) packet. Fortunately, the DS2155 provides separate registers for each controller that will contain information about any errors that occur when receiving data. These registers provide a basis for what action if any the system need to take to continue normal operation.

The HDLC information registers provide on the following receive packet conditions: In Progress, Packet OK, CRC Error, Abort, Overrun, and Message Too Short. The first condition, In Progress, means the HDLC is receiving an packet and no alarms have been detected. Depending on the system, certain actions such as retrieving data from the FIFO may be necessary. The second condition, Packet OK, means the HDLC received a correctly formatted packet, and the data has been checked against the transmitted CRC bytes. The third condition, CRC Error, occurs when the calculated CRC for the received data does not match the transmitted CRC bytes in the packet. The forth condition, Abort, occurs when the HDLC receives the abort signal. The fifth condition, Overrun, occurs when the receive FIFO exceeds the maximum capacity of 128 bytes. This usually indicates the microcontroller did not read the FIFO data faster than the DS2155 writes the received data into the FIFO. The final condition, Message Too Short, indicates that 3 or less bytes including the CRC bytes were received as a message.

Finding the cause of some of the error conditions can be done by simple line testing while others may require in depth knowledge of the system software. When dealing with CRC errors, there are two main causes: either the transmission line is poor quality or there may be problems with the HDLC software/hardware on the transmit or receive side. Testing the line quality is accomplished by performing a bit error rate test while in remote loopback. If the line is not, the problem then further investigation into the HDLC software/hardware is required. The Abort condition is difficult to solve because the cause is most likely on the transmit side which may not be under the designer's control. A common cause is a buffer under run condition in the transmit FIFO which occurs when the transmit HDLC needs to send data, but the processor has not written data into the FIFO. Sometimes, a faster processor will solve the problem, but many times changes need to be made in the software/hardware. The DS2155 has special 'water mark' registers which the processor can use as indicators of the current FIFO status. The 'water mark' registers can be serviced in either a polled mode or can be interrupt driven to ease the processor load. The Overrun condition is caused when the processor does not read data out of the receive FIFO as fast as the receive HDLC writes data into the FIFO. Sometimes, a faster processor will solve the problem, but many times changes need to be made in the software/hardware. The DS2155 has special 'receive packet bytes available' and 'water mark' registers which the processor can use as indicators of the current FIFO status. The 'receive packet bytes available' register is a simple indication of how much data is currently in the FIFO. The 'water mark' registers can be serviced in either a polled mode or can be interrupt driven to ease the processor load. The Message Too Short condition is very easy to deal with; it is used to indicate that the HDLC packet received did not contain enough data and as such is an illegal packet and should be ignored.

Q8. External loopback on the DS26401 or DS2155 does not work properly however, remote and payload loopback work fine?
A8. The cause for this error could be that you are not using the correct source for the Transmit clock (TCLK) in the DS26401. The DS26401DK was designed with three major components: a LIU, a Framer and a FPGA for specific signal muxing. Unfortunately, the receive clock from the LIU goes to the DS26401 and a test point header but not the FPGA. Therefore, to perform external loopback, you need a way to connect RCLK to TCLK.

Solution One: Manually jumper RCLK and TCLK on the DS26401DK with the test point headers. Make sure the TCLK register in the FPGA is tri-stated. This is the default value.

Solution Two: You can control the source on the Transmit clock with TCR3 register (Transmit Control Register) using Bit 4 (TCSS0) and Bit 5 (TCSS1). The following table shows the different options for the transmit clock. Set TCSS0 and TSSC1 to a logic "1". This will cause the Transmit clock to be the same as RCLK from the LIU.

Q9. What are the differences between the DS21455 or DS21458 and the older DS21Q55?
A9. The DS21Q55 is a quad port 27 x 27 mm multi-chip module consisting of four independent DS2155 transceivers. The DS21455 is a monolithic version of the DS21Q55, and is meant to be a drop in replacement that is package, pin, and software compatible. The DS21458 contains

exactly the same die as the DS21455 and is software compatible but it is produced in a smaller 17 x 17 mm package. Note: New designs should use the DS21455 instead of the DS21Q55.

Q10. What is the functional behavior of the RCLK pin output when the signal at the network connection of RTIP/RRING is lost?
A10. When the device looses the signal at the network connection of RTIP/RRING, it enters the carrier loss state. In this state, the RCLK ouput will slowly drift from the recovered clock which is no longer present to the master clock (MCLK) input. Once the network connection is restored, the RCLK output will relock with the signal present on RTIP/RRING.

Q11. When operating T1/E1 devices in T1 mode, can the TCLK pin input frequency be 2.048 MHz?
A11. T1/E1 devices (such as the DS2155, DS21458, and DS26528) provide a wide range of features aimed at easing device configuration. One of these features is the ability of the devices to use a single frequency master clock (MCLK) in either T1 or E1 mode. Unfortunately, the device still requires that the external TCLK pin input be at the actual line frequency. In T1 mode this means the input frequency on the TCLK pin must be 1.544 MHz. However, there are some ways around this limitation, using either the elastic stores for rate conversion, or using the master clock PLL to source TCLK internally at 1.544 MHz.

4. Line Interface Related Questions

Q1. What transformers are recommend for the Dallas Semiconductor devices?
A1. A listing of recommended transformers is provided in application note number 351 and in the last section of the network interface application note number 324.

Both documents are located in the Application Notes section of the Maxim website at www.maxim-ic.com. Just click on the 'APPNOTES' link at the top of the home page and then on the 'Communication Circuits' link.

Q2. What is the function of the capacitor in the transmit path?
A2. The reason that the capacitor exists is to block the flow of current between the TTIP and TRING pins, preventing unnecessary power draw. The capacitor value as stated in the data sheet was chosen such that it appears as a short circuit at the transmission frequency and an open circuit at DC. Although the value is somewhat subjective, this value has been proven to work with all Dallas Semiconductor devices and should not be altered. If the value must be changed, another value can be calculated by the formula f=1/(RC). R is the load as seen by the device (1/4 of the line impedance), C is the capacitor and f is the mean signal frequency. Remember that an all 1s signal appears as a 772 kHz signal and lower 1s density will decrease the signal frequency. The capacitor must be chosen such that the signal frequency is not blocked.

Q3. When using the DS2148 line interface unit in NRZ mode. How should the signals for

the TPOS and TNEG pins be connected?
A3. Connect the NRZ input to TPOS and tie TNEG to ground.

Q4. What is the selection criteria for the Line Build Out (LBO) bits in E1 applications?
A4. It depends not only on the intended application for the Single Chip Transceiver but also what type of system that the design is interfacing to. The line interface circuit can be designed many ways and the following applications explain the difference in the three major operations obtained by switching the line build out. There is also a separate application note available for details on the line interface design.

75/120 ohms normal: This is used for E1 short haul, when the system will used in a confined environment where the return loss is insignificant and the system is not going to be exposed to any lighting surges or power line cross conditions.

75/120 ohm with protection resistors: This is used for E1 long haul, when the system will interact with the outside environment. Here, the return loss is also considered to be insignificant. In order to protect the system from lighting surges and power line cross conditions, power resistors are placed in between the RJ48 connector and the network side of the transformer.

75/120 ohm with high return loss: This is used for E1 long haul, when the system will interact with the outside environment. Here, the return loss is also considered to be significant. In order to protect the system from lighting surges and power line cross conditions, power resistors are placed in between the RJ48 connector and the network side of the transformer.

Q5. When the cable is unplugged for the network interface, why does the Receive Carrier Loss (RCL) bit in the status register or the pin of the Line Interface Unit or Single Chip Transceiver occasionally report an incorrect status?
A5. It is unlikely that the device actually reports the receive carrier loss (RCL) status incorrectly. The most common cause of this problem is that a noise/signal source is coupling into the receive side interface. the RTIP and RRING pins. The following are suggestions to verify that noise/signal coupling is the problem and what can be done to solve the problem.

1. Set the Equalizer Gain Limit (EGL) of the device to the lower of the two settings (i.e. if the two choices are -43dB and -15dB, choose the -15dB setting). This will allow the line interface unit to cut out low level signals that may be causing the device to report the RCL status incorrectly. If this solves the problem, then the EGL bit can be left at this setting for future operation. However, if long haul operation is required by the system, another suggestion should be considered.
2. Set the Transmitter Power Down (TPD) of the device to turn off the transmitter. This will prevent the transmitted signal from coupling into the receiver. If this solves the problem then the problem is more than likely that the transmit TIP/RING signals are too close in proximity to the receive TIP/RING signals. The best solution is to examine the layout of the board and shorten the TIP/RING traces and further separate the transmit and receive signals.

3. Use an oscilloscope to probe the receiver TIP/RING pins when the line is disconnected to observe any noise that may be present. If there is noise on the line with a frequency near the nominal line rate and a large amplitude, then this can be falsely recovered as a signal. The best solution is to examine the board to find the source of the coupled noise and move or shield it from the receiver pins.
4. Use an oscilloscope to probe the power supply directly at the supply pins of the device. If there is noise with an amplitude of 50 mV or greater superimposed on the power supply rail then this can cause problems with the receiver. The best solution is to use decoupling capacitors to filter the power supply to reduce the noise.

Q6. What are the differences between the DS21448 and the older DS21Q48 or DS21Q348?
A6. The DS21Q48 and DS21Q348 are quad port 17 x 17 mm multi-chip modules consisting of four independent Line Interface Units. The DS2148 operates at 5.0 volts and is comprised of DS2148 devices while the DS21Q348 operates at 3.3 volts and is comprised of DS21348 devices. The DS21448 is a monolithic version of the DS21Q348, and is meant to be a drop in replacement that is package, pin, and software compatible. The DS21448 only operates at 3.3 volts and cannot be used as a direct replacement for the DS21Q48.

Q7. Why is the master clock (MCLK) signal necessary for proper device operation?
A7. Because of the hybrid analog and digital nature of the line interface, the master clock signal present on the MCLK pin is necessary to operate both the clock and data recovery engine and the jitter attenuator. Without the master clock, the device would not be able to properly recover the clock and data signal present on the incoming line. The master clock signal is also used as an alternate recovered clock on the RCLK pin whenever device enters a receive carrier loss state. To ensure that the device operates within specification, the master clock should be derived from an accurate low jitter source such as a crystal oscillator. T1/E1 devices usually use a source with a frequency tolerance rating of ± 50 ppm (or better) and a period jitter rating measured in the picoseconds.

Q8. Is the center tap connection of the transformer secondary side necessary for better analog performance on the DS3151, DS3152, DS3153, and DS3154 devices?
A8. Connecting the center tap of the transformer secondary side to the ground is optional. The center tap if used would serve to reduce the common mode noise. However the DS315x devices are all designed to use a coaxial cable connection which has little if any common mode noise. In addition, if the traces between the transformer and the DS315x device pins are short in length, the effects of inductance and common mode noise will be negligible.

5. BERT Related Questions

Q1. When using the DS2155, DS2172, or DS2174 Bit Error Rate Tester (BERT) function with a pseudorandom bit stream (PRBS) pattern, what status bits must be checked to validate that the pattern is being correctly received?
A1. The Status Register 9 (SR9 in the DS2155) should be checked to ensure that the BERT is in

synchronization and that the device is not receiving an all zero pattern. When properly receiving a PRBS patter, the synchronization bit (SYNC or BSYNC in the DS2155) equals 1 and the receive all zeros bit (RA0 or BRA0 in the DS2155) equals 0. When receiving a PRBS pattern it is important to verify that the receive all zeros bit equals 0 since the BERT uses a linear feedback shift register (LFSR) which enters a 'dead state' when it receives all zeros. If the receive all zeros bit equals 1, it is possible for the BERT Bit Counters to begin counting received bits. This would result in the miscalculation of the bit error rate. Therefore, the receive all zeros bit should be checked whenever receiving a PRBS pattern.

Q2. Why do the DS2172 and DS2174 Bit Error Rate Tester (BERT) devices remain in synchronization when the clock signal applied to the receive clock (RCLK) pin is removed or held in a steady state?

A2. Both the DS2172 and DS2174 can remain in synchronization when the clock signal applied to the receive clock (RCLK) is removed. This reason for this behavior is that the state machine which controls the receive synchronization is clocked by the signal applied to the receive clock pin. If the receive clock signal is removed or held in a steady state, the data in the status register will no longer get updated. During this time however, read and write operations will all continue to operate normally. The easiest method to determine if the signal present on the receive clock pin is changing is to read the bit count registers. If the bit count remains the same with each consecutive read, there is no signal on the receive clock pin.

Q3. How is the Latch Count (LC) bit used to set the time interval for the bit and error counters of the DS21372, DS2172, and DS2174?

A3. Both the bit and error counters of the BERT devices contain a second shadow register that is used to latch the current value. When the LC bit is set from 0 to 1, two events occur. First, the current value of the bit and error counters is latched in the shadow registers. Second, the bit and error counters are cleared and will resume operation. The software can then access the shadow registers to read the previous count values. To measure the bit and error counts from time T0 to T1, the following procedure is necessary. At time T0, set the LC bit from 0 to 1. This will clear the bit and error counters and latch the previous count values which can be discarded. At time T1, set the LC bit from 0 to 1. This will clear the bit and error counters and latch the count values from time T0 to T1, which the software can access.

Q4. Why does the DS21372 and DS2172 receive synchronizer sometimes lock to patterns other than the transmitted pattern in repetitive pattern mode?

A4. When the DS21372 and DS2172 are used to generate repetitive patterns, the receiver only searches for a repeating pattern of the same length as the pattern being transmitted. It does not verify the receive pattern matches exactly with the transmit pattern. Once the device has received a pattern of equal length, synchronization is declared. The device will then count any deviations in the received pattern as bit errors. A received pattern of all zeros or all ones will cause the device to synchronize no matter which pattern length is being transmitted. Also, any receive pattern length which is an even divisor of the transmit patter length will cause the device to synchronize. Consider the following examples which meet the criteria above.

Transmit pattern	10111000	Original Pattern Programmed into Device
Receive pattern	10111000	Device Synchronizes to Correct Pattern
Receive pattern	00000000	Device Synchronizes to Wrong Pattern
Receive pattern	11110000	Device Synchronizes to Wrong Pattern
Receive pattern	10101010	Device Synchronizes to Wrong Pattern

After synchronization is established, the software should check the pattern receive registers to verify that the correct pattern is being received. Also, the receive all zeros and received all ones indicators the status register can be used for pattern verification.

6. HDLC Related Questions

Q1. What are the differences between Bridge and Configuration mode in the HDLC controller?
A1. Configuration mode allows only the local bus to control and monitor the chip while the HDLC packet data will be transferred via the PCI bus. Data cannot be passed from the local bus to the PCI bus in this mode.

Bridge mode allows the host on the PCI bus to access the local bus. The PCI bus is used to control and monitor the chip and transfer the packet data. Data can be mapped from the PCI bus to the local bus.

Q2. Does the DS31256 HDLC controller support 8 bit local bus mode?
A2. Yes, the 8 bit local bus is available in bridge mode and has 2 distinct PCI functions.

Function 0:
Allows read and write operations to the DS31256 registers through the PCI bus using 8 or 16 bits wide access. However, this function does not allow access to the DS31256 registers which perform read and write operations on the local bus.

Function 1:
Allows read and write operations from the PCI bus to the local bus. The software must configure the LBW bit in the LBBMC register to define the width of the local bus as 8 or 16 bits wide.

Q3. How is the absolute address calculated in DS31256 or DS3131 HDLC controller?
A3. The The absolute addresses, also known as the real addresses or machine addresses, is a fixed address in memory. The absolute address is the base address plus the actual address being used by the device. For proper operation, the absolute address has to be allocated correctly when configuring the DMA controller in the device. The equation for calculating the absolute address is:

Absolute Address = Base Address + Actual Address in Use

For example consider the DS31256 HDLC Envoy controller Receive Done Queue End Address being used by the device. The actual end address is not an absolute address. If the base address is 0x10000000 and the receive done queue end address is 0x400. The calculation is:

0x10009000 + 0x400 * 4, and the absolute address is 0x1000A000.

7. Design Kit Related Questions

Q1. How can I get the most updated definition files for the T1E1DK?
A1. These files are available from the Dallas Semiconductor applications support group. The definition files may be obtained by requesting them from telecom.support@dalsemi.com

Q2. What software is available for Dallas Semiconductor design kits?
A2. The software used with the Dallas Semiconductor design kits is known as ChipView. ChipView is a PC based demonstration program that is used to interact with Dallas Semiconductor's T/E carrier design kits. The program has been written such that it may be used to control all T/E carrier design kits that utilize either a serial or USB port. ChipView has three basic modes of operation, Demo Mode, Register View, and Terminal Mode.

Demo mode provides a high level user interface for configuring the device registers on the daughter cards using radio buttons and menu selections. The current device status for functions such as LOS, OOF, and AIS is displayed with easy to read widgets. This interface is meant to make device configuration as easy as possible.

Register View provides an intuitive user interface for reading, writing, and viewing the individual device registers on the daughter card. The device registers are displayed by name in an on-screen array and the values can be changed using the keyboard or mouse. This interface provides complete control of every bit and function of the specific device.

Terminal mode provides direct access to the design kits processor. The list of all recognized commands is listed when the user types "help" or "?" at the command prompt. This mode is for low level debugging of the daughter card and should be reserved for seasoned users.

Q3. What device design kits are currently available through Dallas Semiconductor?
A3. There are two kinds of design kits available from Dallas Semiconductor. The first type is a stand alone design kit which contains the computer interface circuitry and the evaluation device. The second type is a combination mother board and daughter card. The mother board contains the computer interface circuitry and the daughter card contains the evaluation device. The DK101 mother board is a low cost version which supports a single daughter card. The DK2000 mother board is a high performance version which supports multiple daughter cards.

The following devices have stand alone design kits available:
DS21349, DS2149, DS2174, DS21Q50, DS21Q55, DS21Q58, DS21Q59, DS21Q352, DS21Q354, DS21Q552, DS21Q554, DS31256, DS3131, DS3150, DS3153, DS3154

The following devices have daughter card design kits available:
DS21352, DS21354, DS2155, DS2156, DS21Q348, DS21448, DS21455, DS21458, DS26401, DS3112, DS3144

More Information

DS21348:	QuickView	Full (PDF) Data Sheet	Free Samples
DS2148:	QuickView	Full (PDF) Data Sheet	Free Samples
DS2155:	QuickView	Full (PDF) Data Sheet	Free Samples
DS21Q352:	QuickView	Full (PDF) Data Sheet	Free Samples
DS21Q354:	QuickView	Full (PDF) Data Sheet	Free Samples
DS21Q552:	QuickView	Full (PDF) Data Sheet	Free Samples
DS21Q554:	QuickView	Full (PDF) Data Sheet	Free Samples